

Ultra-Fast Multi-Frame Mega-Pixel Imager for Proton Radiography

Kris Kwiatkowski for

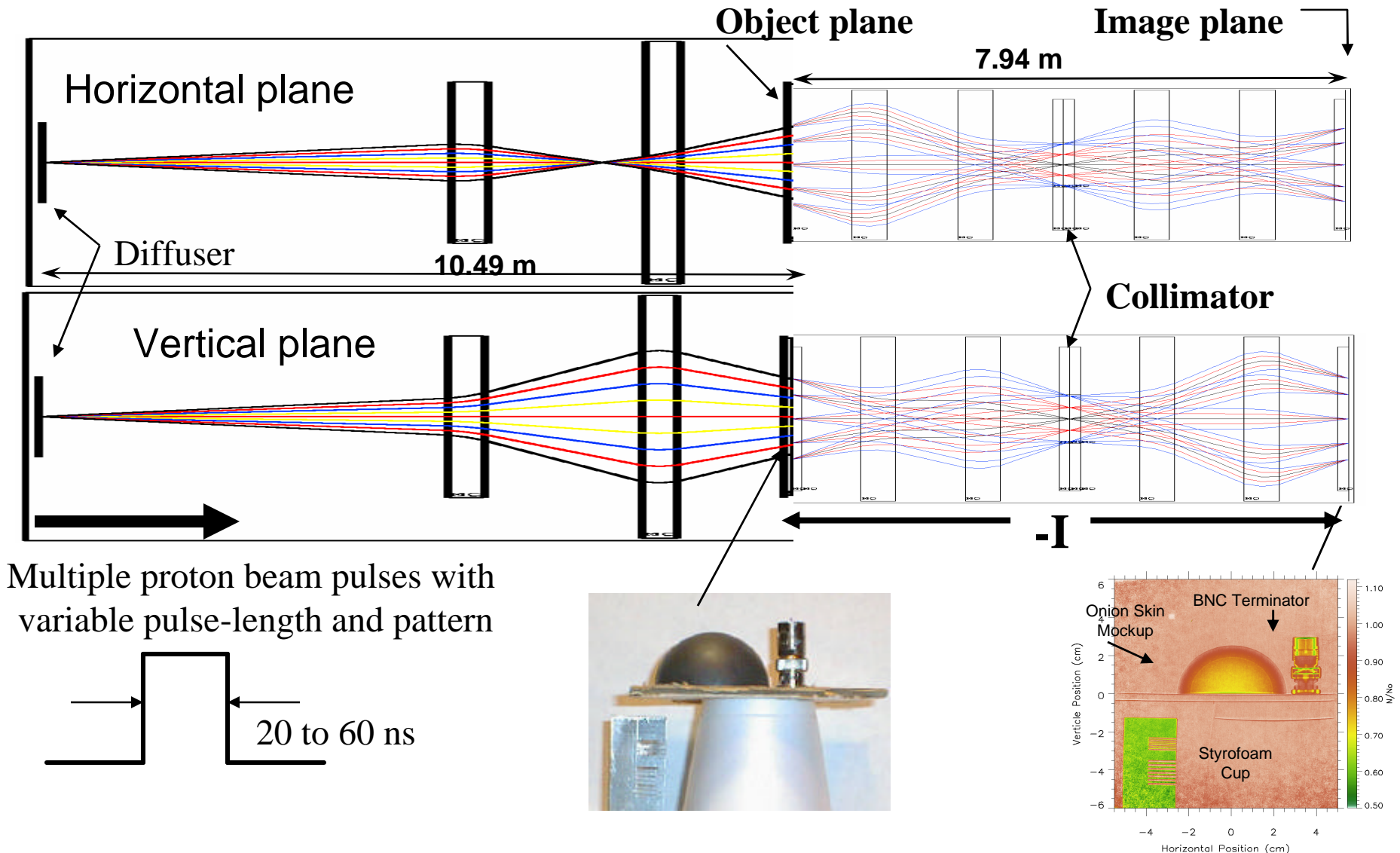
LANL, Rockwell Scientific, GE - Global Research,
AFRL Kirtland and University of California – Irvine
Collaboration

LSST FPA workshop BNL, February 2004

Overview

- Proton Radiography and requirements
- Few frame imager (Rockwell)
- Ultra- Fast Imager/ “streak camera”
- Work on Multi-Frame Imager interconnect technologies

Magnetic Lens for pRAD

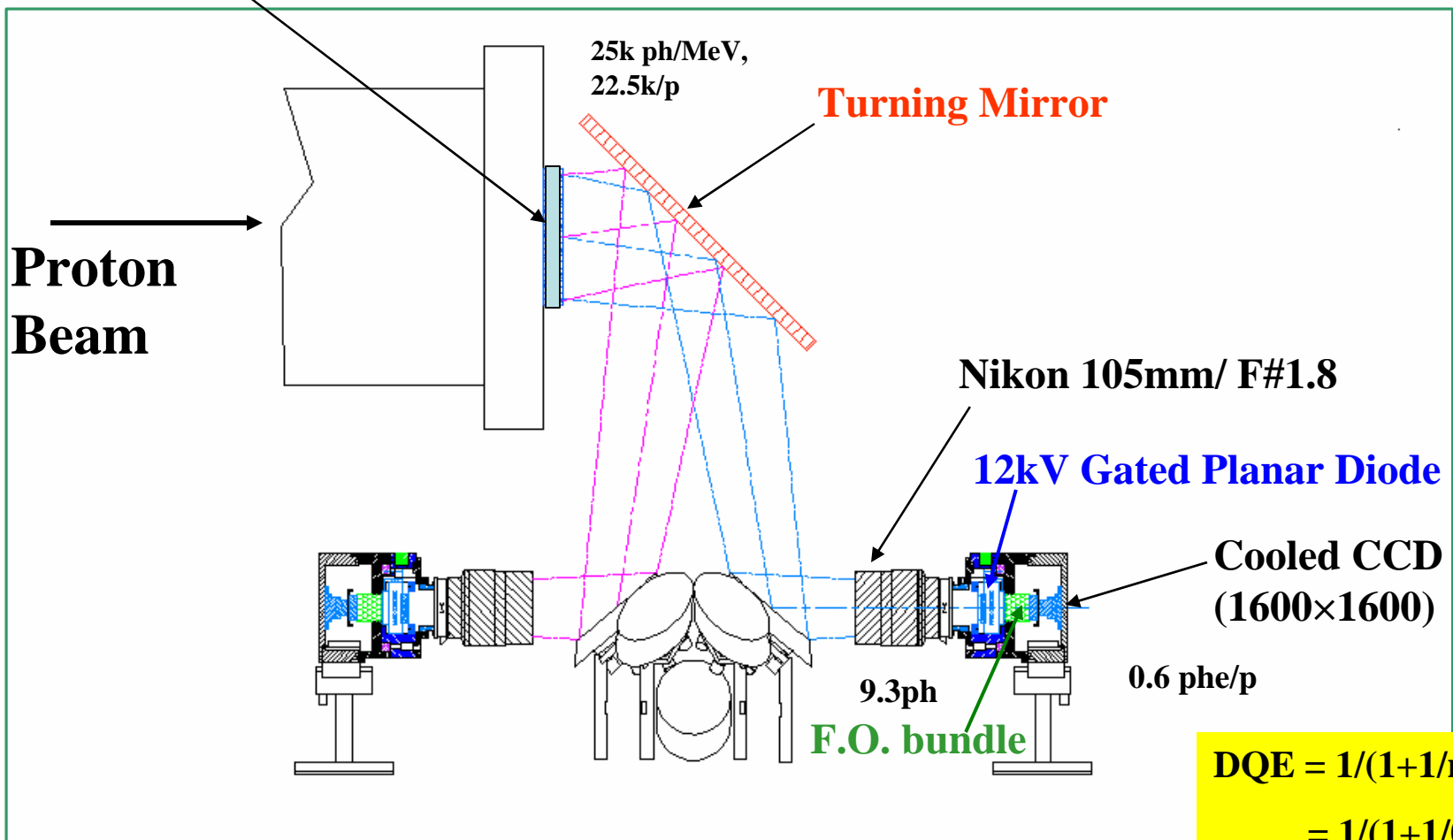


Proton Radiography 7-CCD Camera System

1-2 mm thick LSO-scintillator

Mosaic 12cm×12cm (black backing)

Resolution $\geq 2.5\text{lp/mm}$
($\leq 200\mu\text{m}$)



$$\begin{aligned} \text{DQE} &= 1/(1+1/n) \\ &= 1/(1+1/0.6) \\ &= 0.4 \end{aligned}$$

Limitations of Gated CCD Imagers

- Number of frames = 7 (one CCD per frame)
- Limited resolution and DQE due to:
 - bi-planar diode photo-cathode QE ~15%
 - fiber bundle-to-CCD chip coupling
 - radiation ? light ? phe's ? light ? phe's in CCD
- Long range blur
- 12kV H.V. pulsers
- Complexity and maintenance cost

Requirements for pRAD Imager

- Number of frames: 32 (64 goal)
- Optical Fill Factor: $> 90\%$
- Inter-frame time: 200 ns
- Array Size: $> 1024 \times 1024$ pixels
(2 – 4Mpx)
- Dynamic Range: 11 bits (12-bits)
- Well depth up to: $\sim 10^6 e^-$
- QE $> 75\%$ (at 415nm)

Considered Three Imager Technologies

- **Fast CCD's** – w/ electronic shuttering: problems w/ asynchronous shutter, $\sim 1\text{Me-}$ well depth, QE in blue, pixel count, fill factor (trade-off w/ storage) (Princeton, Sarnoff, Summit, LL/MIT, Etoh,...)
- Monolithic **CMOS APS** (back-illuminated APS ??)
 - fill factor, low QE, shutter ratio, large pixels
- *****Hybrid Imager** (photo-sensor + CMOS ROIC)
optimal solution, but still issues with interconnect, and Si area limitations for storage of large number of frames

Hybrid FPA: A High Performance Approach

- Independent optimization of detector and readout IC
- ~100% optical fill factor
- Large well depth

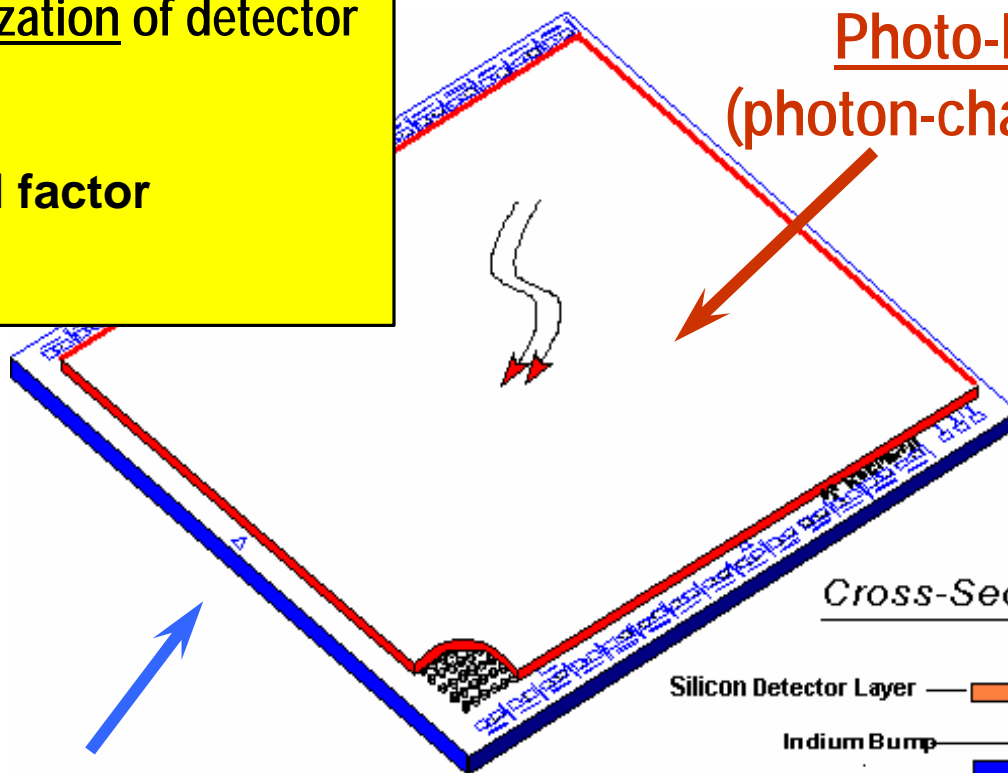
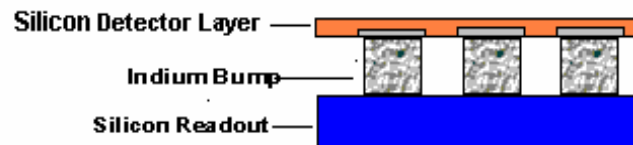


Photo-Diode Array
(photon-charge conversion)

Cross-Sectional View



CMOS Readout IC (charge-voltage conversion & signal processing, including A/D; SoC: photons-to-bits)

200-ns Inter-Frame Imager Challenges

- All pixels have to be processed in parallel (~Mpx)
 - each pixel needs independent FE electronics
 - burst mode: w/ analog storage, SCA, space “intensive”:
MiM caps $0.8 \text{ fF}/\mu\text{m}^2 \Rightarrow 64 \times 200 \text{ fF} = \underline{126 \times 126 \mu\text{m}^2}$
 - OR real-time A/D conversion (space, BW, digital noise)
- Deliver bias to center of Si-sensor, and power and ground to CMOS ROIC (~100% occupancy and 200 ns rep. rate)
- Sensor – to – ROIC interconnect & packaging (redundancy vs. repairability)

Interim and Long Term Solutions

- **3-frame imager in fabrication:**
 - analog storage, 2Mpixel, 26 μ m pixels; SF front-end, and CDS per pixel;
 - 2-D flip-chip architecture; 1440 \times 1440 pixels, 38 \times 38 mm² format >> standard CMOS reticle size ? requires either tiling or reticle stitching
- **In parallel: develop basic technologies for Multi-frame imager: CMOS electronics, interconnect, photo-sensors** (in collaboration with other National Labs, Universities and Industry R&D Centers)

Rockwell Fast Imager

(specs as in the initial contract)

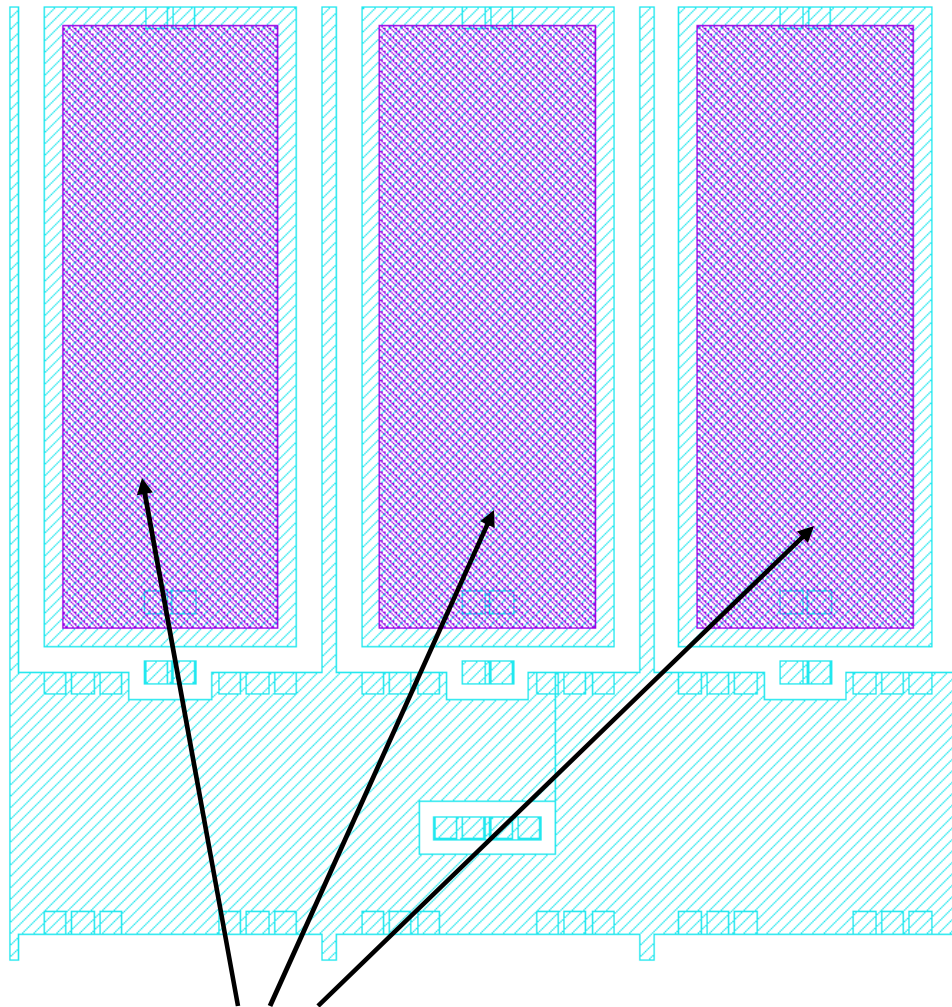
- Number of stored frames: 1
- Array Size: 1024×1024 pixels (1Mpx)
- Pixel size: 18μm × 18μm
- Electronic snap-shot shutter
- Minimum integration time: 180ns (358 ns)
- Fill Factor = 100%, QE > 75% at 420nm
- Extinction ratio better than 1: 60,000
- Dynamic Range: 11 bits (12-bit nominal)

Rockwell Imager Upgrade

(modified contract)

- Number of stored frames: 3
- Array size: 1440×1440 pixels (2Mpx)
- Effective Die size: 39×39 mm²
- Pixel size: 26μm × 26μm
- Electronic snap-shot shutter
- Minimum integration time: 180 ns (358ns)
- Fill Factor = ~94%, QE > 80% at 420nm
- Full readout in 12ms
- Dynamic Range: 11bits (12-bit nominal)

Rockwell Imager 26 μ m Pixel Layout



3 MiM Storage Caps

Tiling Approach

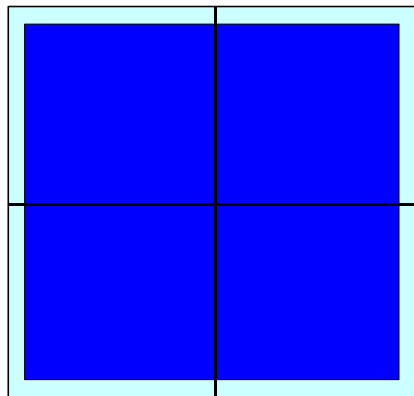
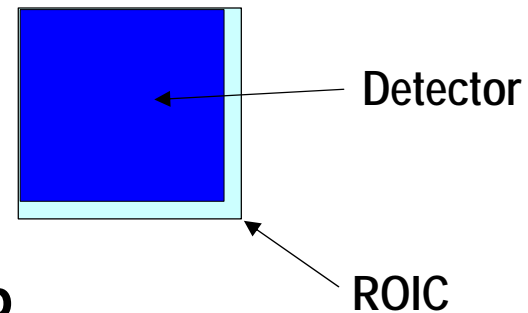
Phase-1: Single Chip (2-side buttable)

Edge distance: ~ a few pixels

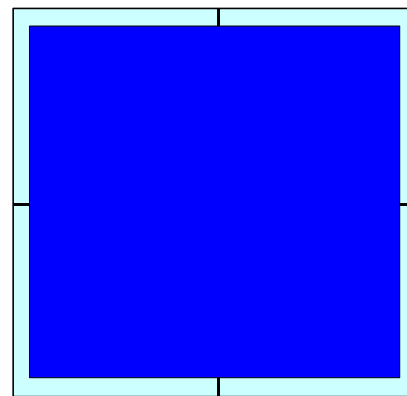
Phase-2: Mosaic Chip

Four-chips tiling: gap ~ a few pixels OR

Single-sensor and CMOS tiled: gap ~ a few pixels (challenging)

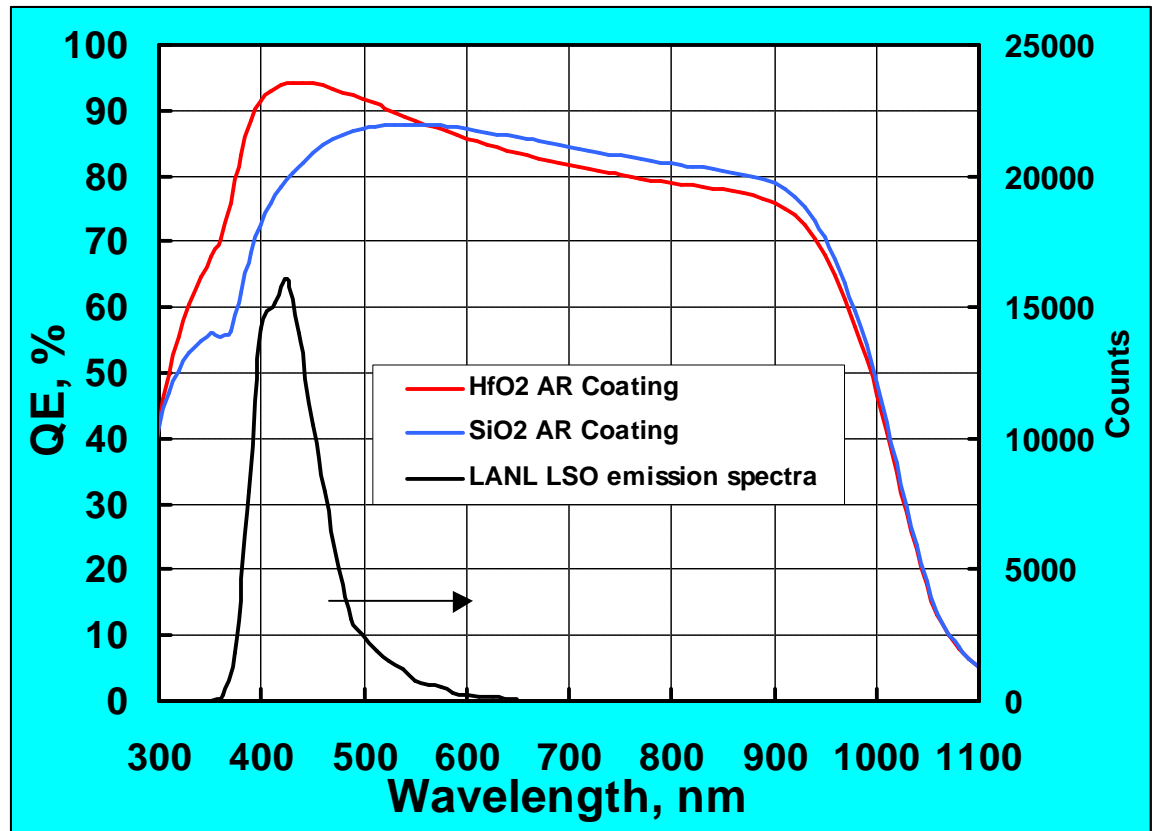


OR



Spectral QE Simulation

- Standard SiO_2 -based ARC can meet 75% peak QE at 420nm
- HfO_2 coating material can achieve peak QE >90% @420nm



3-Frame Imager Status

- Most effort focused on ROIC electronics, so far
 - 0.25 μ m CMOS (UMC foundry)
 - design phase was followed by detailed parasitics extraction and v. extensive pixel and system simulations
 - noise and DR within the specs (ADC limited !)
 - well depth 190ke-, w/ PGA gain adjust; (0.6Me- option)
 - “tape-out” was in mid January 2004
 - detector layout: for now tiling (future- reticle stitching)
- Photo-sensor design & tiling evaluation are underway
- Camera housing, trigger logic, computer interface (~done)

Rockwell Imager Status

Critical Design Review July 28, 2003; four external experts:
BNL, Univ. of Arizona, and LBNL + LANL and Rockwell groups
Very valuable: directly and indirectly uncovered some problems,
3½ months of follow up work (mostly the ADC)

RSC is re-using existing IP from other projects – CMOS building blocks (control logic, line drivers, ADC,...) - while this practice saves cost, it ties new IC to older design and foundry process, cannot be optimized for specific application

LANL contract office – “stop work” => 3 weeks delay and at least \$5k in cost (maintaining good communications helps)

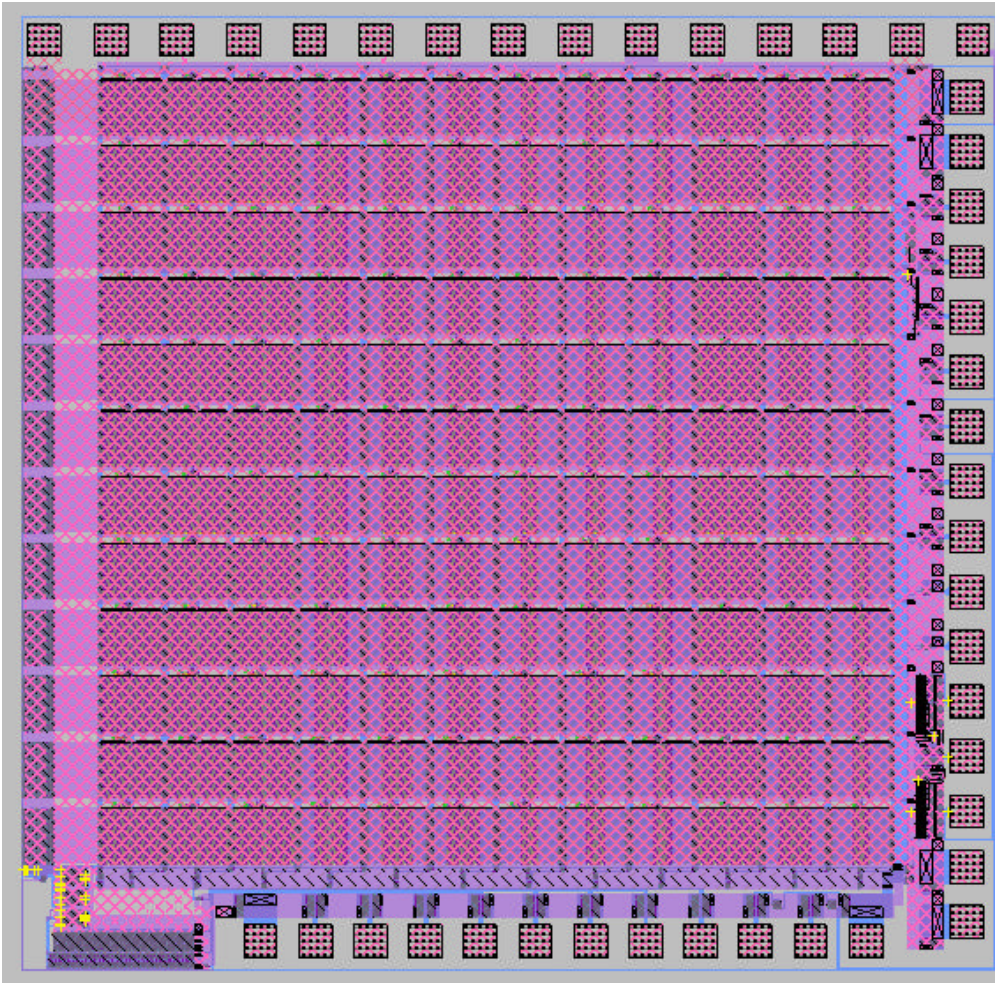
Technology Development for 32/ 64-Frame Imager

Two main areas (enabling technologies):

- Fast and Ultra-Fast CMOS FEE
(Univ. of California – Irvine)
- Interconnect and Packaging
 - develop “affordable” interconnect schemes
 - 3-D vertical stack of test chips (GE - cube)
 - 3-D FPA and ROIC integration (μ -machining)

5 M-Frame/s Imager Chip

developed at Univ. of California - Irvine

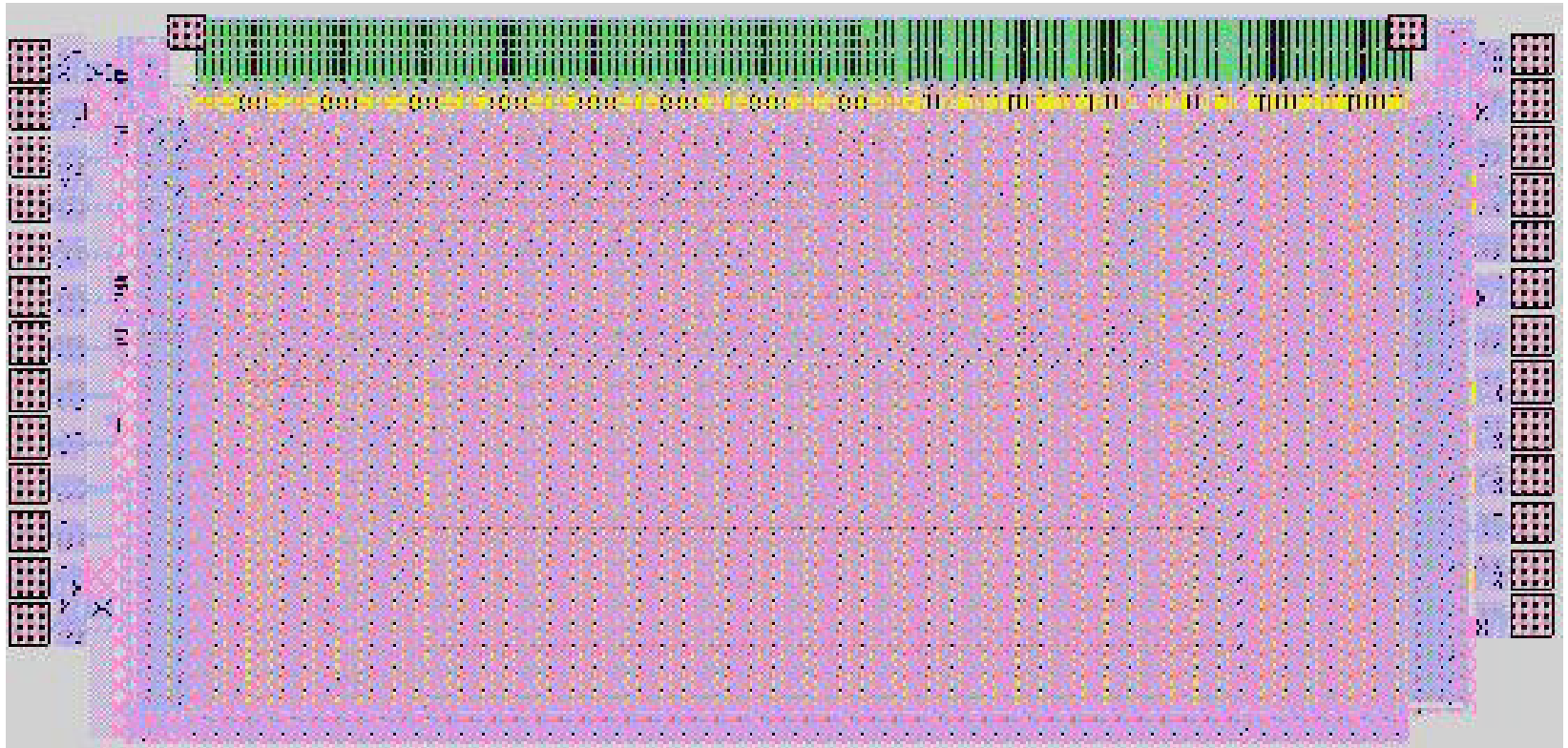


- 5 M-frames/s
- ~13 bits SNR.
- 64 frames per pixel memory
- Correlated double sampling
- 12×12 array

“UC-I MegaCam1” Chip Performance

- 0.35 μm CMOS TSMC, $200 \times 200 \mu\text{m}^2$ pixels.
- Photo-diode + charge integrating amp and sample/hold array / pixel.
- 32-frame storage with CDS, 64 without.
- 5 to 7- μW DC power consumption per pixel.
- Over 4 M-frame/s (250 ns) with CDS, 7-MHz (145 ns) without CDS.
- S/N is ~13 bits, RMS. \Rightarrow exceeds specs

Solid State Streak-1 - Layout (UC- I)



- 0.35 μm CMOS, @ 20 μm pitch, two-row staggered
- 150 pixels wide by 150-samples deep

Streak1 Performance

- Max measured acquisition speed: 400 MHz (2.5ns)
- Readout speed: 10 MHz
- Photodiode area: 3500 square microns
- Photodiode fill factor: 92%
- Photodiode capacitance: ~0.4 pF
- Fixed pattern noise: 6 mV, rms
- Temporal noise: 0.512 mV, rms
- Dynamic range: 69.2 dB, rms (11.5 bits, rms)

Proposed: *GigaCam*

- = **400 M-frames/s** operation with 8+ bits
- Possibility of up to ~1 GHz.
- ~50 μm pixel pitch with ~16 frames / pixel.
- CIF (352 x 288 pixel) or larger form factor.
- Fast, low power A/D converters per pixel or per sample, fast digital readout, with all data converted and read out in well under 1 ms.
- Would achieve over 50 T-Pixels/s acquisition speed and over 1 G-Pixels/s readout speed.

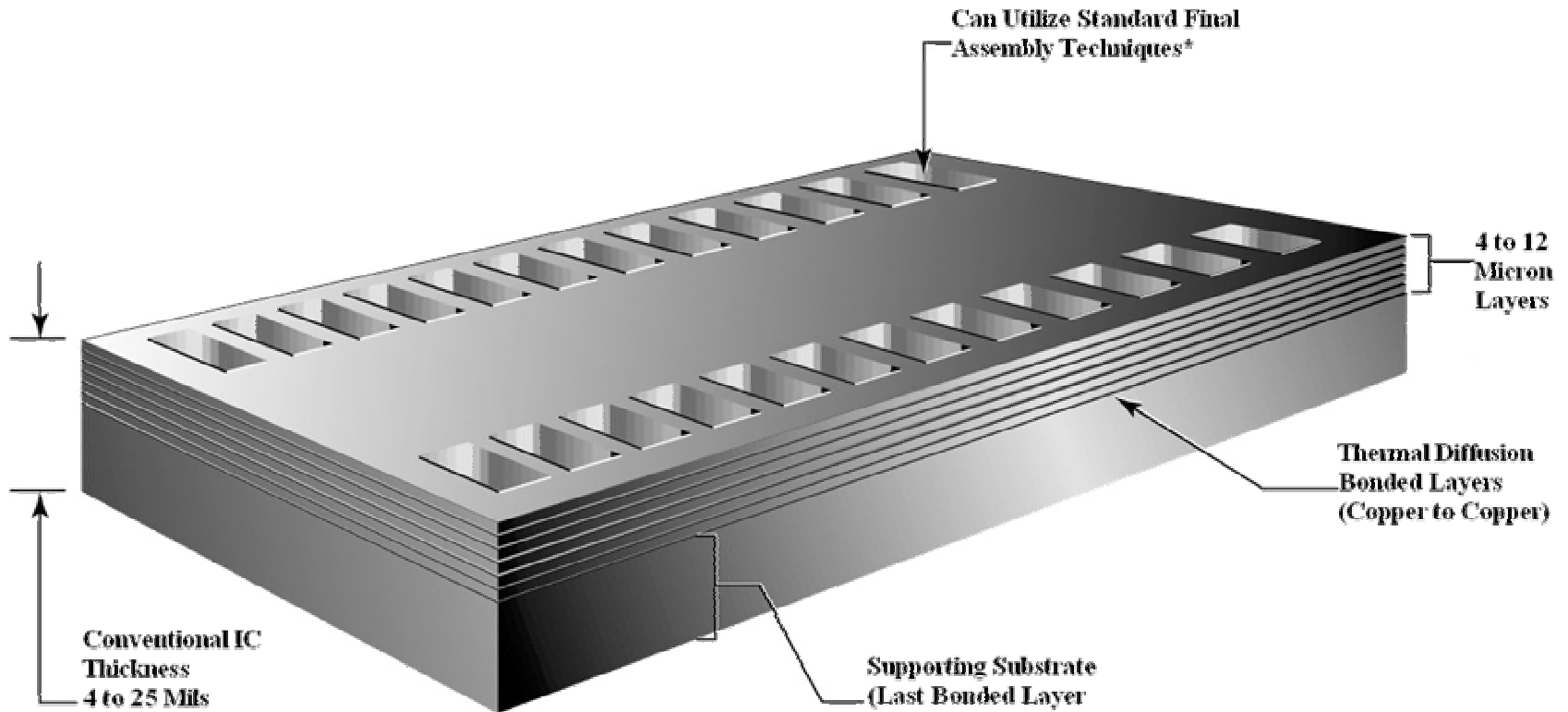
Interconnect Architecture options for 32-frame imager

Even in 0.18 μm CMOS, and reasonable ($\sim 30\mu\text{m}^2$) pixel Si pitch, the pixel footprint inadequate to accommodate storage and FEE

Options:

- 2-D (flip chip) w/ very large pixels $\sim 120 - 200\mu\text{m}$
(v. large detector $1024 \times 0.12\text{mm} = 12.3\text{cm}$)
- 3-D “horizontal” wafer stacking with thru-Si vias
(limited Si-area gain, vias, emerging technology)
- 3-D vertical (edge-on) stack (deck of playing cards)

Example of 4-to-7 Layer Monolithic 3-D Stack



Stacking on wafer level by Tachyon Semiconductor

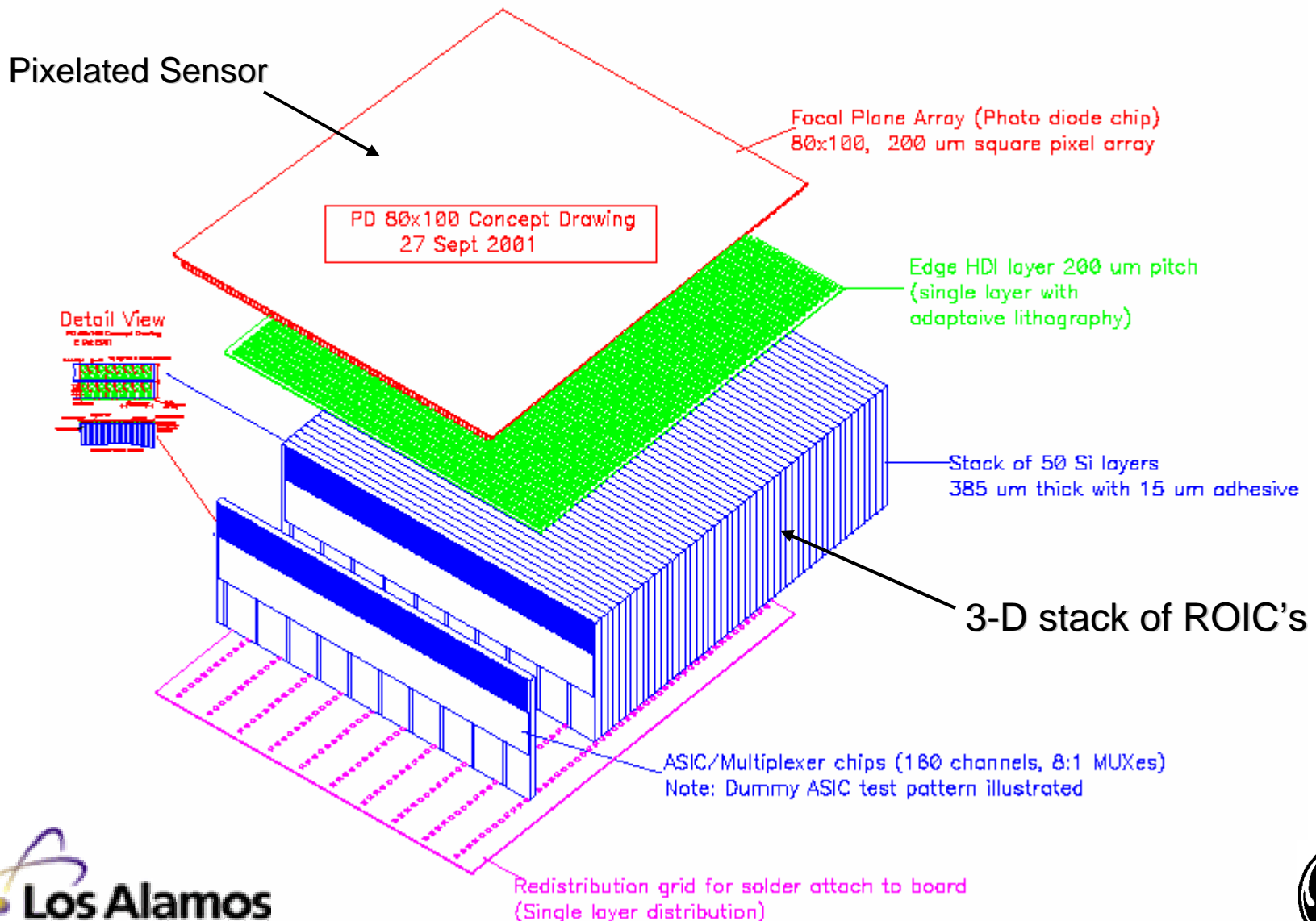
Tachyon Semiconductor

Interconnect for 32-frame Hybrid Imager

LANL, AFRL and GE-R&D Center

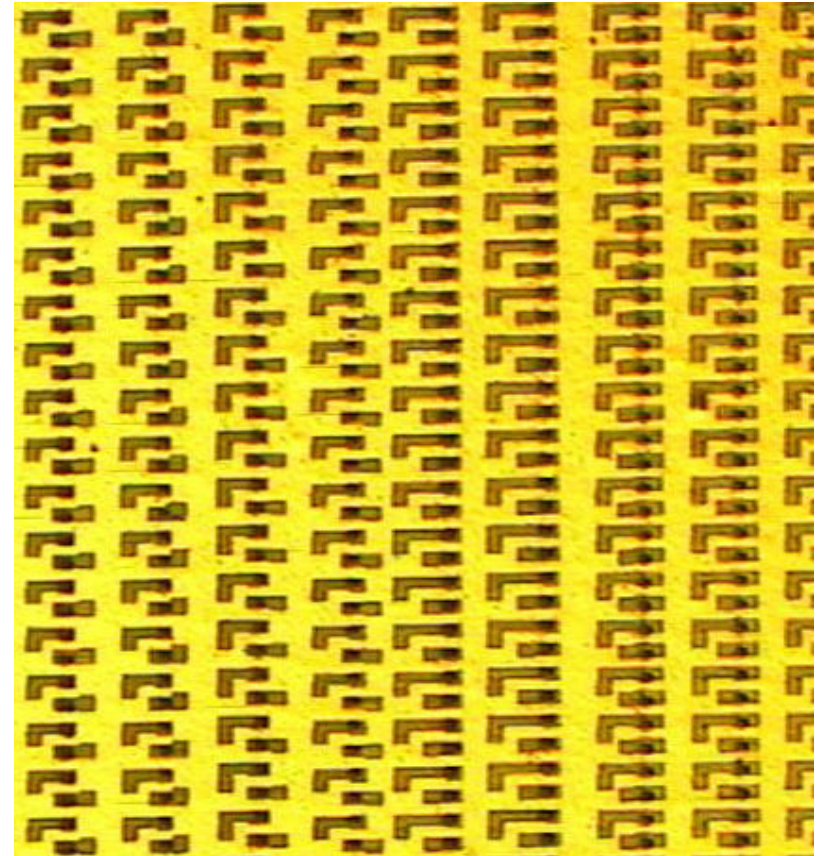
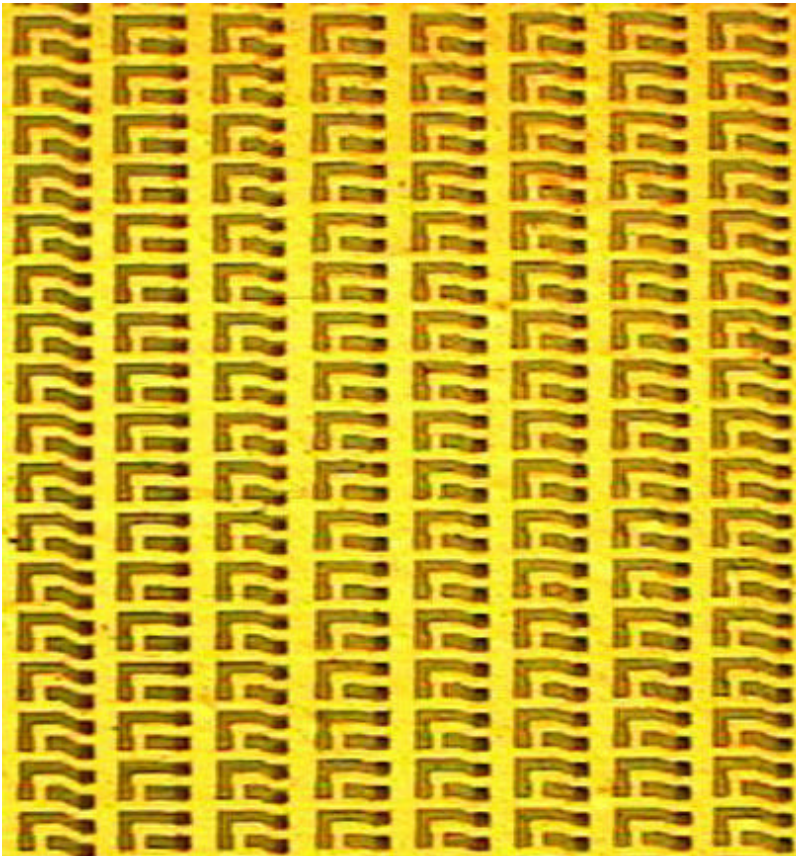
- 3-D vertical stack of ROIC chips
- Built 50-chip stack (8000 interconnecting bumps on top, 750-I/O to bottom PWB layer)
adaptive lithography, conductive polymer bumps and gold studs
- Continuity interconnect only, some problems on the periphery/ corners

Imaging Cube Concept

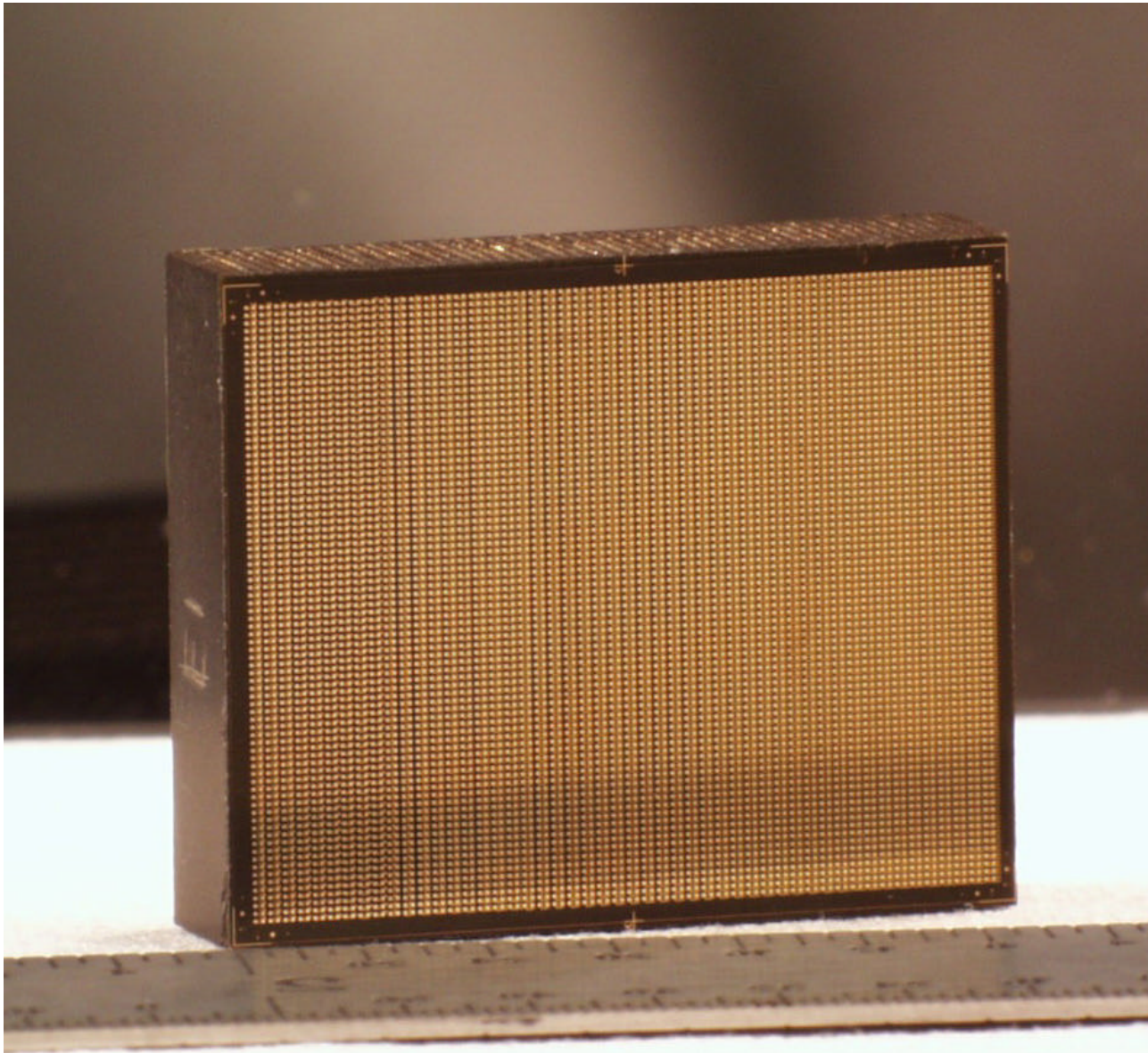


Top (8000 I/O) HDL Layer -1: MT1

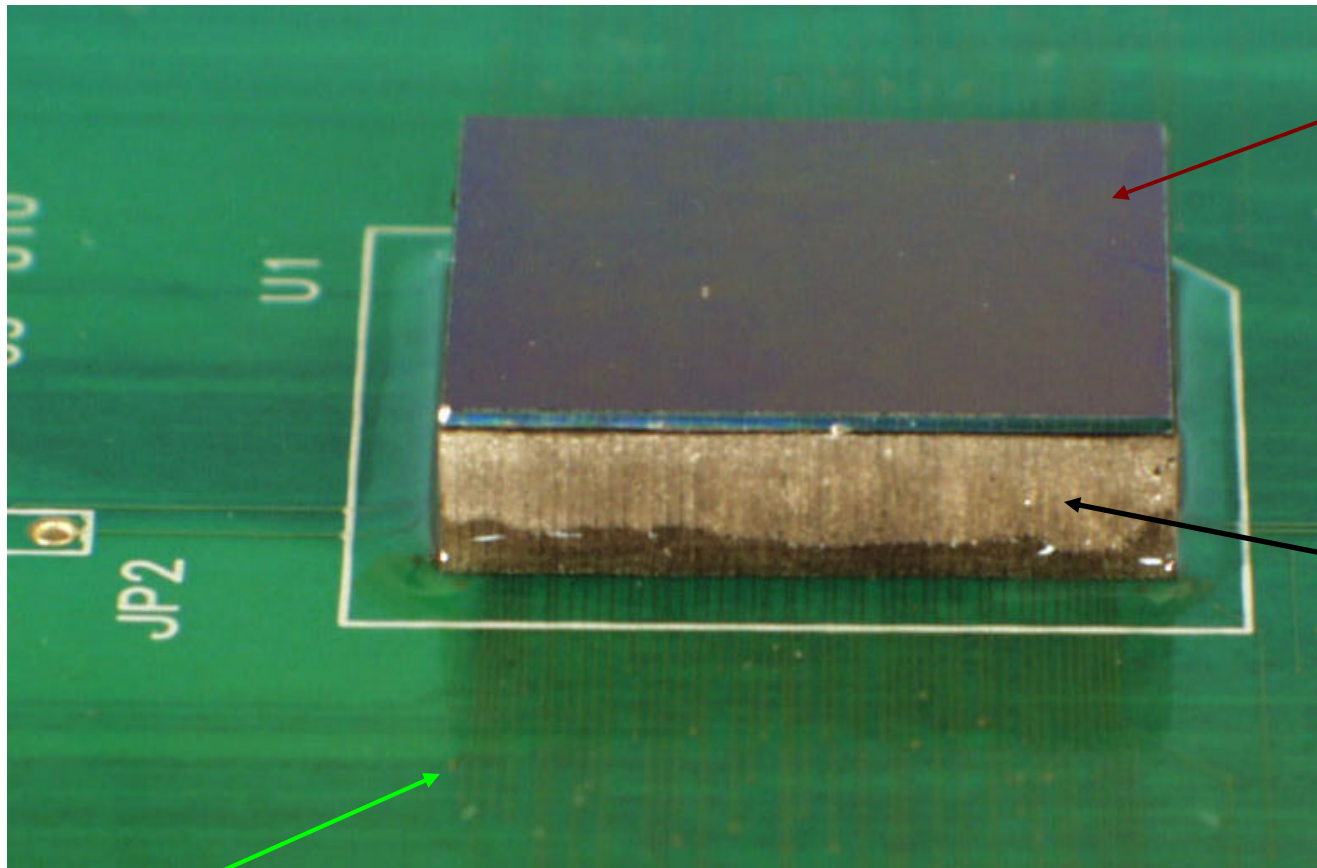
Adaptive Lithography at Work



Cube – Close-Up

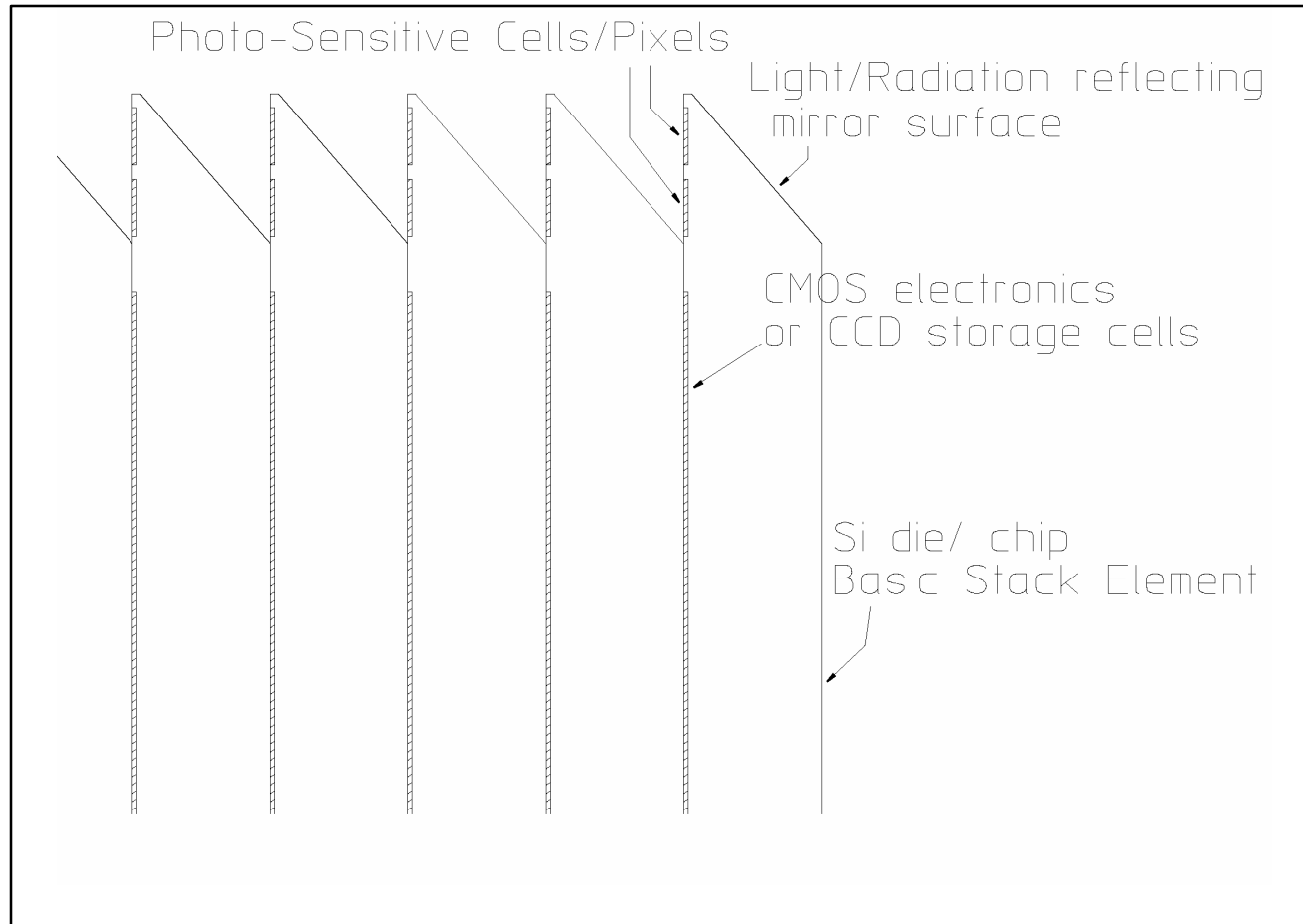


Finished Cube w/ FPA Bump Bonded



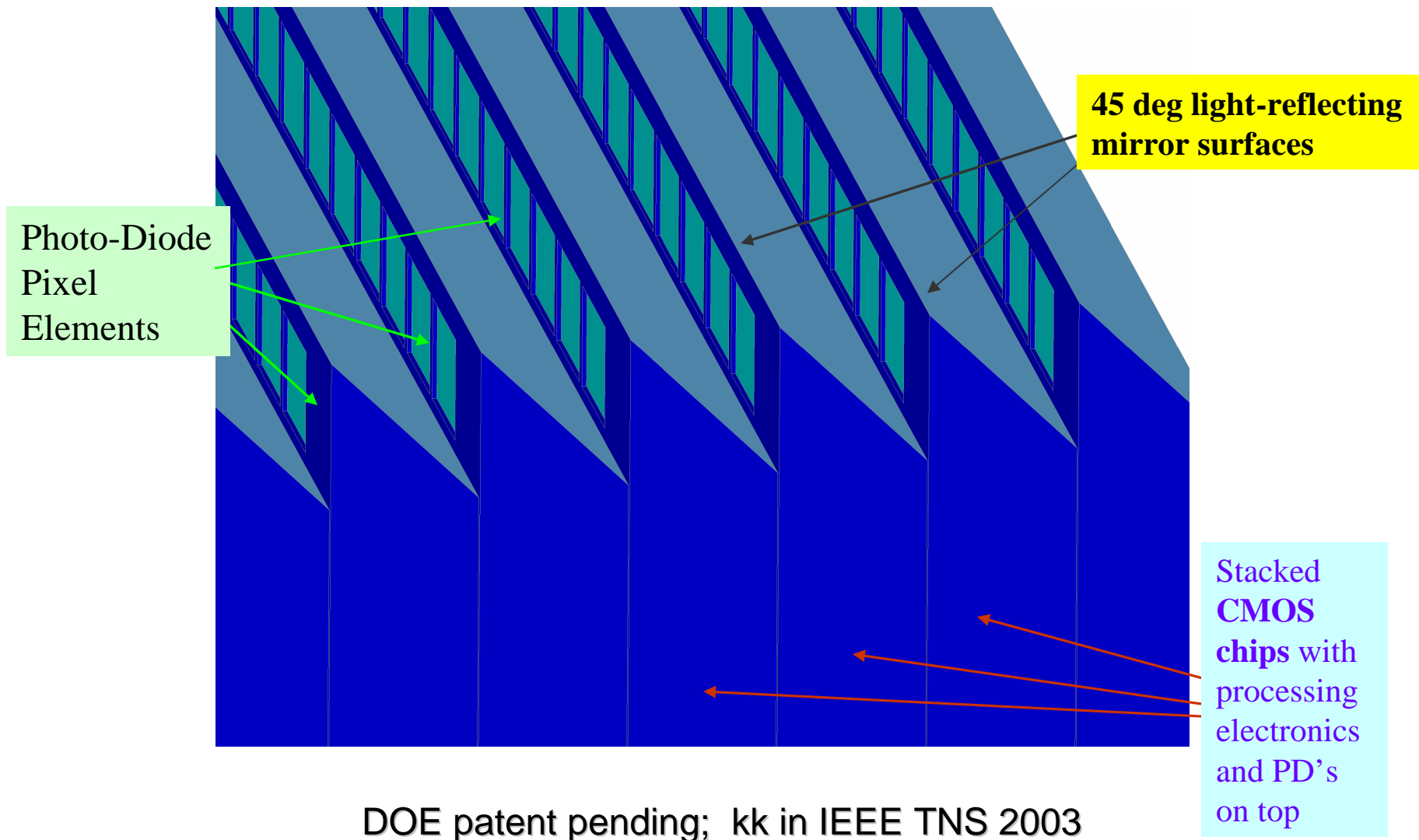
PCB test board

Sensor Integrated into CMOS Electronics in 3-D Vertical Stack



DOE patent pending; IEEE TNS 2004

Integrated Sensor & CMOS Electronics in 3-D Vertical Stack



CMOS Active Pixel **CID** Sensor:

An aside – new CID for Multiple Readouts?

SPECIFICATIONS:

- 2048 x 2048 resolution
- 12 μ m square pixels
- 5V / 0.18 μ m CMOS process
- Preamp / pixel architecture
- On-chip, 2048 parallel CDS

KEY PARAMETERS:

- ~250ke- pixel capacity
- < 15e read noise @ 4 MHz
- < 8e dark current @ -36C
- > 40% QE @ 540nm (front side)

FEATURES:

- Random pixel addressing
- Non-destructive readout
- Selective ROI clearing
- Built-in anti-blooming
- 10⁸ dynamic range using Auto-Integrate Software

Summary

- CMOS+hi resistivity-Si 2Mpx sensor hybrid detector in fabrication; 5MHz frame rate, full r/o in 12ms
- System noise 90e- (DR 11-bits, limited by ADC)
- Burst mode operation w/ 3-frame analog storage
- ROIC (actually SoC) tiled; future - reticle stitching
- 4MHz and 100MHz 64-frame FE demonstrated with 13/10-bit DR (Univ.Cal-Irvine--)
- 3-D interconnect enabling technology for high-density, massively parallel systems, e.g. Imaging Cube

3-D Packaging Benefits and Challenges

- Design evolution towards integration of sensor, electronics and packaging
 - allow, e.g. multiple amps to select for min. $1/f$ noise; or for space applic. - on-chip data compression
- Known Good Die (KDG)
- Power dissipation
- Repairability
 - self-test, and redundancy
 - intelligent (self)-reconfigurable system